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MOCA ARM: Analog Reliability Measurement based on Monte Carlo Analysis

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ABSTRACT

Due to the expected increase of defects in circuits based on deep sub-micron technologies, reliability has become an important design criterion. Although different approaches have been developed to estimate reliability in digital circuits and some measuring concepts have been separately presented to reveal the quality of analog circuit reliability in the literature, there is a gap to estimate reliability when circuit includes analog and digital structures. In this paper, we propose a new classification method using Monte Carlo analysis to calculate the reliability of analog circuits and show its efficacy when it is used for a combination of analog and digital circuits. Our method is based on signal reliability concepts and measures the probability of passing correct or faulty values. Furthermore, we compare our reliability measurements with the reliability definitions come from other failure mechanisms in sub-micron technologies. Simulation results show the reliability measurement presented here which provides key information for reliability improvement and monitoring.

1. INTRODUCTION

Although the continuous reduction in scaling of integrated circuits lead to powerful, fast and more complex devices, it causes some serious problems such as high power consumption, current leakage and parametric variations. Many of these challenges lead on to degradation in the reliability of devices. The reliability of a circuit is a measure of its susceptibility to different faults [1], which is a major concern for high-density circuits in deep micron technology.

The challenges in reliability and failure analysis of portable electronic products and micro-electro-mechanical systems (MEMS) conduct to a new research studies. In some previous studies, the reliability prediction and assessment depends on the origin of failure mechanisms, hence the mathematical reliability model for each single failure mechanism has been presented in [2].

Reliability concept for analog circuits has been addressed for different types of faults such as permanent, intermittent and transient faults. Because of various types of faults and failure mechanisms, the unified evaluation of analog reliability is not easy especially when the circuit includes digital and analog parts related to each other. The reliability measurement of only digital circuits has been presented in [1]. Furthermore, authors in [3] showed how to improve the resiliency and hardening of digital circuits by some techniques such as triple-modular redundancy (TMR) applied on the sensitive nodes of digital circuits. To show the efficacy of the applied hardening methods, it is important to measure the reliability before and after hardening. Whereas after applying hardening method especially with analog block insertion, the reliability measurement becomes a challenge.

In this paper, we present an analog reliability measurement based on failure probability and Mont Carlo analysis that we called as MOCA ARM, to calculate analog reliability with the ability of applying on mixed analog and digital circuits and show its efficiency by simulation results.

The rest of this paper is organized as follows: Section 2 reviews some important previous efforts carried out on analog reliability. Section 3 presents the signal probability algorithm for analog reliability and shows the simulation results of the proposed method. Section 4 indicates the capability of our method to cover previous works. Finally, section 5 concludes the paper.

2. Previous Works on Analog Reliability Measurements

Different factors affect the reliability of semiconductor devices including temperature, hot-carrier degradation (HCD), time-dependent dielectric breakdown (TDDB), negative-bias temperature instability (NBTI) and electro-migration (EM), which change lifetime and failure rate.

Temperature effect on lifetime is expressed by the following equation [4].

$$L = A\exp(\frac{Ea}{KT}) \quad (1)$$

where, lindicates life time, *T* is absolute temperature, *A* is a constant, *Ea* is thermal activation energy (in eV) and finally *K* is Boltzmann's Constant (8.63 × 10-5 eV/°K).

For other failure causes, failure rate is usually measured by mean time to failure factor [5] which depends on the type of failure. The overall relation between failure rate (λ), reliability (R) and mean time to failure (MTTF) is shown in (2) in which the reliability is measured by an Arrhenius's general formula [6].

$$\mathrm{R} = \exp(-\lambda \mathrm{t}), \quad \mathrm{MTTF} = \int \mathrm{R(t)}\,\mathrm{dt} = \frac{1}{\lambda} \quad (2)$$

MTTF depend on the type of failure mechanisms. Equations (3), (4), (5), and (6) indicate MTTF based on TDDB failure mechanism [7], degradation induced by hot-carrier[7]]-[[8], NBTI phenomenon [7] and electro-migration failure mechanism [7], [9] respectively. Table 1 shows the abbreviations of the parameters of these equations

$$MTTF_{TDDB} = A_{TDDB}\frac{A_g}{V_{gs}^{\alpha-\beta T}}\exp(\frac{X}{T}+\frac{Y}{T^2}) \quad (3)$$

$$MTTF_{HCD} = A_{HCD}\exp(\frac{\theta}{V_{ds}}) \quad (4)$$

$$MTTF_{NBTI} = A_{NBTI}(\frac{1}{V_{gs}})^{\gamma}\exp(\frac{Ea}{KT}) \quad (5)$$

$$MTTF_{EM} = A_{EM}(J\times T)^{-n}\exp\frac{Ea_{EM}}{KT} \quad (6)$$

TABLE 1
ABBREVIATION OF PARAMETERS IN FAILURE MODELS

Parameter	Unit	Description
AHCD and θ		Constants determined from life testing
Vds	V	Drain-Source Voltage
ATDDB		Empirical constant
α, β, Y, X		Fitting parameters
Ag	m2	MOSFET gate oxide area
Vgs	V	Gate-Source Voltage
T	°K	Absolute temperature
ANBTI		Process-related constant
γ		Voltage acceleration factor 6–8
AEM		Empirical constant depending on the cross-sectional area
Ea	eV	Thermal Activation Energy
K	eV/°K	Boltzmann's constant (8.63 × 10-5)
J		Current density
n		Material and failure mode-dependent scaling factor (n = 2: refer to J. R. Black)

3. of MOCA ARM Definition, Motivation and Simulation Results

A. MOCA ARM definition and motivation

MOCA ARM presented in this paper is an analog reliability measurement analysis based on Monte Carlo simulation to measure a mixed of analog and digital circuit reliability before and after hardening with a unique methodology. In this methodology, we defined the signal reliability of each node as the probability of generating correct or expected value. This definition is the same for analog and digital signals and helps us to measure the circuit reliability improvement after inserting analog blocks in comparison with the digital circuit without hardening.

In the literature, there are some analog blocks inserted on sensitive nodes to mask transient faults and harden the whole circuit. Fig. 1 shows a technique to reduce the magnitude of transient pulse presented in [10] which works based on two serial transmission gates. In this structure, the second transmission gate is four times larger than the first in size. Fig. 2 shows a Schmitt trigger circuit which mainly applied to eliminate chattering in convertors and its hysteresis property [11]. As shown in Fig. 3, authors in [12] have used the masking property of Schmitt trigger and the pass transistor gates to build an efficient analog block for hardening of combinational logics against soft error. When a signal with a moderate transient pulse enters to the proposed circuit, the circuit efficiently eliminates error at the output. All of these analog blocks can be applied to a digital circuit in order to

improve its reliability and MOCA ARM method can evaluate the reliability of sensitive nodes before and after hardening.

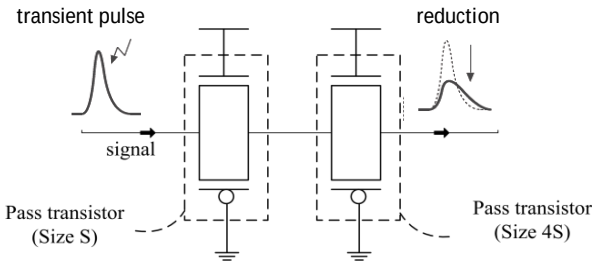

Figure 1: Using pass transistors for reducing the magnitude of transient pulses [10].

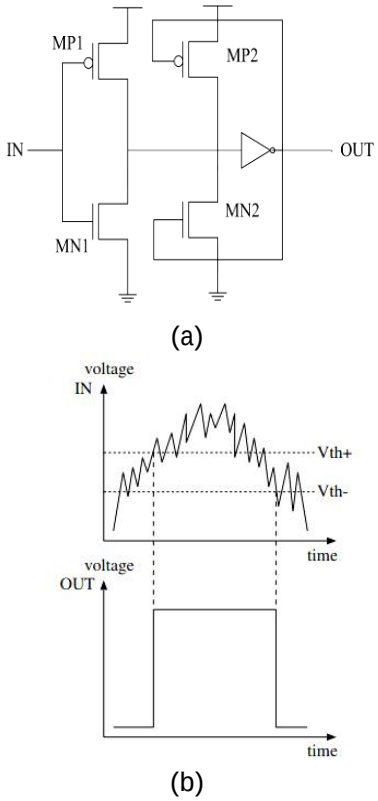

Figure 2: (a) Schmitt trigger circuit; (b) Hysteresis property of schmitt trigger circuit [11].

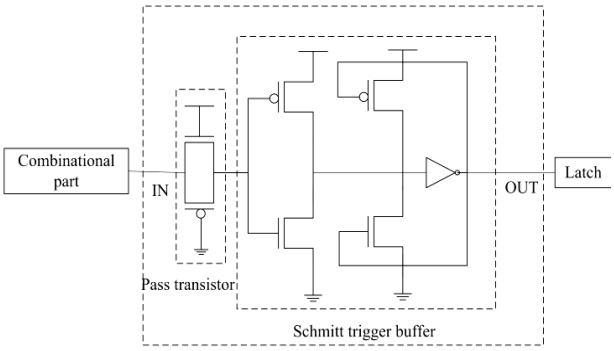

Figure 3: Soft error masking circuit [12].

We consider the analog reliability in MOCA ARM as the failure probability of the signal. Assume that a binary signal x can take four different values: correct zero (0_c), correct one (1_c), incorrect zero (0_i), and incorrect one (1_i). Then, the matrices are completed by probabilities for occurrence of each one of these four values as shown below [13]:

$$\begin{bmatrix} P(x=0_c) & P(x=1_i) \\ P(x=0_i) & P(x=1_c) \end{bmatrix} = \begin{bmatrix} x_0 & x_1 \\ x_2 & x_3 \end{bmatrix} \quad (7)$$

The signal reliability for x, noted R_x, is defined as the probability of producing correct or expected values and come from 8.

$$R_x = P(x=0_c) + P(x=1_c) = x_0 + x_3 \quad (8)$$

The probability of correct and incorrect values is evaluated in SPICE by injecting exponential current pulse in sensitive nodes, mimicking a particle-induced soft error transient and Monte Carlo analysis.

B. Simulation results

In the simulation, we design every circuit in a TSMC 45nm CMOS technology and 1V supply voltage. HSPICE Monte Carlo simulation carried out with 30 sweeps. Besides Schmitt trigger circuit, we consider a rising input threshold voltage Vth^+=0.8 V and a falling input threshold voltage Vth^- =0.2 V. We use circuit C17 as our test vehicle example from ISCAS'85 benchmark [14] which is shown in Fig. 4.

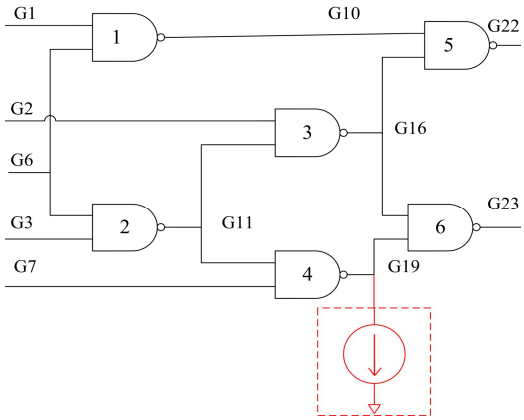

Figure 4: C17 from ISCAS'85 combinational benchmark circuits.

To show the efficacy of MOCA ARM, we apply different types of hardening methods on C17 sensitive nodes induced by a particle strike, which is modelled by an exponential current source [15] and evaluate the reliability of nodes before and after hardening.

$$I(t) = I_0(\exp(-t/\tau_\alpha) - \exp(-t/\tau_\beta)) \quad (9)$$

where I_0 is the charge injected current of the particle strike, τ_α is the collection time constant of the junction and τ_β is the time constant for initially establishing ion trap. In this paper, value of τ_α and τ_β in simulations are respectively set to 164ps and 50ps, such as performed in [15].

We calculate x_i as the failure probability according to 7 for example, x_0 is defined as:

x_0=Number of correct values/Total number of iterations (10)

To calculate x0, we apply the inputs of C17 in a properly manner so that the sensitive node gets a '0' logic value, then apply a current source to model induced transient fault. We simulate the circuit by applying a current source, as shown in dashed line in Fig. 4, with the mean amplitude value 30mA and a standard deviation 20mA in 30 Monte Carlo runs and evaluate the corresponding probability failure. The proper circuit setup is carried out to evaluate x1, x2 and x3 failure probabilities separately. Table 2 shows the improvement of the circuit reliability after adding Schmitt trigger circuit at node G19 and Table 3 is the same as Table 2 repeated for node G22.

TABLE 2
ANALOG RELIABILITY IMPROVEMENT WITH SCHMITT TRIGGER AT NODE G19

	x0	x1	x2	x3	R
C17	0.20	0.77	0.80	0.23	0.43
C17+ Schmitt (G19)	0.83	0.20	0.17	0.80	1.63

TABLE 3
ANALOG RELIABILITY IMPROVEMENT WITH SCHMITT TRIGGER AT NODE G22

	x0	x1	x2	x3	R
C17	0.6	0.73	0.4	0.27	0.87
C17+ Schmitt (G22)	0.67	0.6	0.33	0.4	1.07

In these tables, R is the reliability before and after hardening. As shown, the reliability after hardening increases and accepts a value between zero and two because it provided by the summation of two probabilities (x0, x3). The results of Tables 2 and 3 show that the reliability increase after hardening. To demonstrate the feasibility of our proposed method to the accurate estimation of hardened circuit's reliability, we apply three hardening methods on node G22, and compare their reliabilities with each other. The results are shown in Table 4. As the simulation set of Table 2, assume that a soft error transient zero fault occurred on node G22. First row shows G22 reliability before hardening, the other rows show the reliability of the circuit after hardening by only pass transistor, only Schmitt trigger and the combination of pass transistor and Schmitt trigger, respectively. The reliability results are arranged in a bar graph shown in Fig. 5. As shown in the graph, we can increase the robustness of the circuit in node G22 by applying pass transistor, Schmitt trigger and mixed method respectively. The best reliability, measured by MOCA ARM, is achieved by the mixed method.

TABLE 4
ANALOG RELIABILITY IMPROVEMENT WITH DIFFERENT HARDENING METHODS AT NODE G22

	x0	x1	x2	x3	R
C17	0.6	0.73	0.4	0.27	0.87
C17+pass transistor	0.6	0.67	0.4	0.33	0.93
C17+Schmitt trigger	0.67	0.6	0.33	0.4	1.07
C17+Schmitt trigger + pass transistor	0.8	0.47	0.2	0.53	1.33

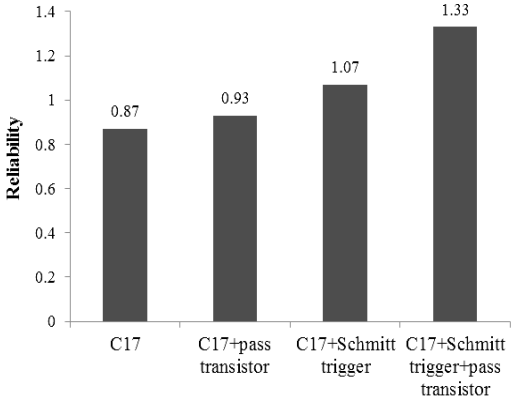

Figure 5: The comparison of Analog reliability for different hardening methods

4. MOCA ARM CAPABILITIES TO COVER PREVIOUS METHODS

To show the efficacy of MOCA ARM and its compatibility with the failure mechanisms' equations expressed in section II in evaluation of analog reliability, we investigate temperature, area and drain-source voltage effects on the proposed reliability calculations. To show the effect of temperature on the reliability of C17, we add Schmitt trigger which is shown in Fig. 6 to harden node G22 and measure the node reliability before and after hardening on three different temperatures.

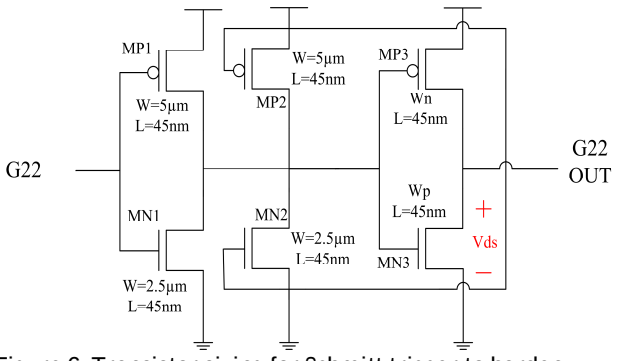

Figure 6: Transistor sizing for Schmitt trigger to harden node G22

The results is organized in Table 5 and compared by a bar chart presented in Fig. 7. The bar chart exposes the reduction of reliability when temperature increases, which approve the drop of reliability based on (1), (3), (5), (6). Furthermore, Fig. 7 shows the growth of reliability after hardening by Schmitt trigger in each temperature.

TABLE 5
TEMPERATURE EFFECTS ON RELIABILITY

	T	x0	x1	x2	x3	R
C17	25°C	0.73	0.76	0.27	0.24	0.97
	35°C	0.6	0.83	0.4	0.17	0.77
	50°C	0.33	0.96	0.67	0.04	0.37
C17+ Schmitt(G22)	25°C	0.77	0.27	0.23	0.73	1.50
	35°C	0.76	0.5	0.24	0.5	1.26
	50°C	0.53	0.7	0.47	0.3	0.83

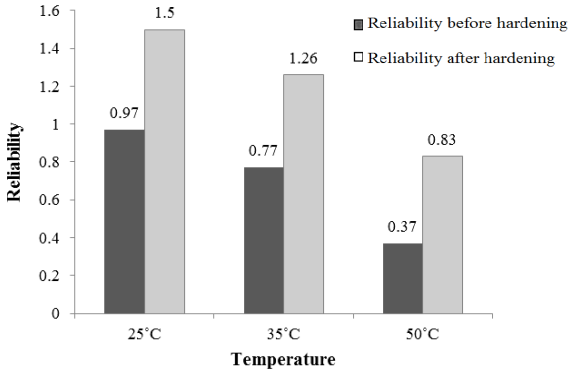

Figure 7: The comparison of temperature effects on reliability

To reveal the area changing impact on reliability emphasized in MTTF-TDDB equation, we increase the capacity of the Schmitt trigger output node which is added to node G22 to harden C17.

We expanded the width of the Schmitt trigger output inverter transistors as reported in Table 6 and investigated its effect on the resiliency of C17. Fig. 8 which is provided by Table 6 data, shows the larger area improves the reliability of circuit. This outcome is well-suited by (3) in which by increasing the area the MTTF and reliability are increased.

TABLE 6
IMPACT OF AREA ON RELIABILITY

C17+Schmitt(G22)					
The dimension of inverter (l=45nm)	x0	x1	x2	x3	R
Wn=45µ, Wp=112.5µ	0.40	0.93	0.60	0.07	0.47
Wn=50µ, Wp=125µ	0.87	0.80	0.13	0.20	1.07
Wn=55µ, Wp=137.5µ	1	0.47	0	0.53	1.53

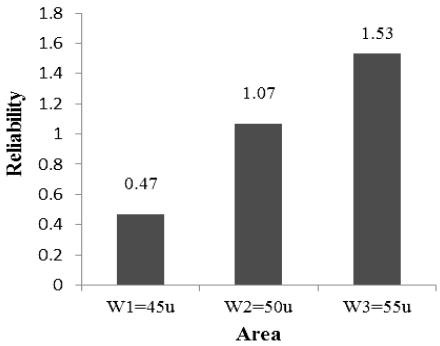

Figure 8: Reliability for three designs with increasing additional area requirements

Besides the mentioned capabilities, MOCA ARM supports the reliability based on MTTF-HCD expressed in (4). To show its compatibility, we slightly change the value of Schmitt trigger input node (G22) by adjusting the values of C17 inputs in a way that the proposed node keeps its logical value in suitable range of Vth+ and Vth-. In this condition, we slightly change the drain-source voltage of NMOS transistor in Fig. 6. As reported results in Table 7, the reliability of node G22 increases by the slightly drop in Vds which is compatible with the calculation of reliability based on (4).

TABLE 7
IMPACT OF DRAIN-SOURCE VOLTAGE ON RELIABILITY

C17+Schmitt(G22)					
Vds	x0	x1	x2	x3	R
999.9075 mv	0.77	0.13	0.23	0.87	1.64
848.7851 mv	0.83	0	0.17	1	1.83

The summation of the presented simulation results show the compatibility of our analog reliability measurement based on Monte Carlo analysis method with expressions which have been mentioned previously to estimate MTTF and reliability.

5. CONCLUSION

This paper shows the efficacy of applying signal probability as a valid indication of the reliability evaluation of hardened combinational circuits with analog blocks. Our analog reliability measurement to calculate the reliability is based on Monte Carlo analysis and estimates the failure probability of the circuit nodes. The simulation results, designed in TSMC 45nm CMOS technology, exhibited the capability of the proposed method to evaluate reliability before and after applying the analog blocks to digital circuits. Moreover, the results show MOCA ARM method is robust against changing important parameters previously mentioned for MTTF and analog reliability such as temperature, area and drain-

source voltages; hence it is a feasible and efficient method for analog reliability measurement.

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